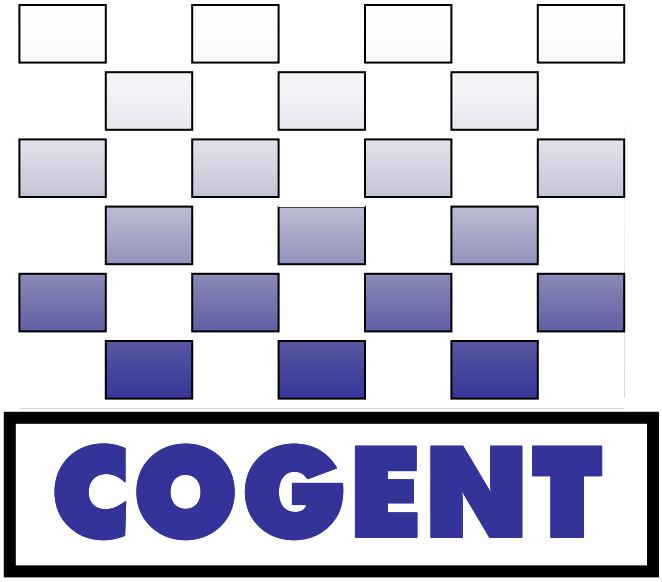

Cogent CSB1724
Marvell 88F6282
System On a Module (SOM)

Hardware Reference Manual

Cogent Computer Systems, Inc.

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1 WARRANTY

The enclosed product ("the Product"), a part of the Cogent Single Board series, is warranted by Cogent Computer Systems, Inc. ("Cogent") for a period of one year for reasonable development, testing and use, all as further described and defined below. This warranty runs solely to the individual or entity purchasing the Product and is not transferable or assignable in any respect. This warranty is valid only for so long as the product is used intact as shipped from Cogent. Any attempt or effort to alter the Product, including but not limited to any attempt to solder, de-solder, unplug, replace, add or affix any part or component of or onto the Product, other than components specifically intended for the user to plug and unplug into appropriate sockets and/or connectors to facilitate user programming, development and deployment, all as specifically described and authorized in this Product Hardware Reference Manual, shall void this warranty in all respects. Coverage under this warranty requires that the Product be used and stored at all times in conditions with proper electrostatic protection necessary and appropriate for a complex electronic device. These conditions include proper temperature, humidity, radiation, atmosphere and voltage (standard commercial environment, 0C to +70C, <60%RH). Any Product that has been modified without the express, prior written consent of Cogent is not covered by this warranty. The use or connection of any test or bus connector, adapter or component with any device other than a Cogent connector or adapter shall void this warranty and the warranty of all other components, parts and modules connected to the rest of the system. Cogent shall not be responsible for any damage to the Product as a result of a customer's use or application of circuitry not developed or approved by Cogent for use on or in connection with the Product.

This warranty does not cover defects caused by electrical or temperature fluctuations or from stress resulting from or caused by abuse, misuse or misapplication of the Product. Any evidence of tampering with the serial number on the Product shall immediately void this warranty. This Product is not intended to be used on or embedded in or otherwise used in connection with any life sustaining or life saving product and this warranty is not applicable nor is Cogent liable in any respect if the Product is so used. Notwithstanding anything to the contrary herein, Cogent expressly disclaims any implied warranty of merchantability or implied warranty of fitness for a particular purpose in connection with the manufacture or use of the Product.

2 OPERATING SPECIFICATIONS

2.1 CSB1724 OPERATING SPECIFICATIONS

The CSB1724 conforms to the following specifications:

Specification	Value
Dimensions	70mm x 50mm x 5.7mm (no Heatsink on 4.3mm Socket)
Weight	~30g
Storage Temperature	-20C to +100C
Operating Temperature	0C to +70C (requires application specific thermal solution)
Humidity	0% to 95% RH, Non-Condensing
Input Voltage (VIN)	+8V to +24V, Nominal +12V
Output Voltage (VCC3)	+3.3V +/- 10%, 4A Maximum
IPM Voltage (VCC3SB)	3.3V +/- 10%, <100ma Maximum
Power Consumption	1.5W Typical, 3W Maximum

Table 1 – CSB1724 Operating Specifications

3 OVERVIEW

3.1 INTRODUCTION

The CSB1724 was designed and developed by Cogent Computer Systems, Inc. as a highly integrated Marvell 88F6282 System On a Module (SOM). The CSB1724 provides a small, powerful, flexible engine for embedded control systems of all kinds. The major features of the CSB1724 are as follows:

- **CPU** - 1.6Ghz 88F6282 Sheeva ARMv5TE Core
- **CACHE** - 16KByte Instruction and Data Caches; 256KByte L2 Cache
- **SDRAM** – 1GByte 16-Bit Wide DDR3-800 Memory
- **FLASH** - On-Board 512MByte SLC NAND
- **PCI EXPRESS** - Two PCIe 1.1 Links (x1)
- **GIGABIT ETHERNET** - Two 10/100/1000 ports via Dual RGMII to Copper PHY
- **SECURITY** - On-Chip Cryptographic and Security Acceleration Engines Supporting: AES128; DES/3DES; MD-5 and SHA1 hashing; and others
- **XOR/RAID** - High Speed XOR DMA Engine for RAID Storage Applications
- **SATA** - Dual SATA Gen 2 (1.5Gbit or 3Gbit/sec) Channels
- **USB** - Two 480Mbit USB 2.0 Host Ports via On-Board HUB
- **SERIAL I/O** - 2-wire TTL UART, I2C, SPI and I2S Audio Ports
- **SD/MMC** - 4-Bit SD/MMC Port (SDIO Compliant)
- **JTAG** - Standard ARM JTAG (Header located off module)
- **OPERATING VOLTAGE** - 12V Input Rail; On-Board 3.3V (with 3 Amp available to off board devices), 1.8V (SDRAM), 1.0/1.1V (CPU) Power Supplies
- **POWER MANAGEMENT** - On-Board ATXMEGA Microcontroller for Power Sequencing, Voltage Monitoring and Boot Configuration
- **OPERATING TEMPERATURE** - 0C to +70C Standard
- **POWER CONSUMPTION** - 3W typ., 4W Max, <10mw Standby
- **COGENT NETWORK SOM COMPLIANT** - Common, Interchangeable Footprint across Multiple CPU Architectures (x86, PowerPC, MIPS and ARM); Low Cost Industry Standard MXM-II Socket
- **ULTRA COMPACT SIZE** - 70mm x 50mm x 5.7mm (using 4.3mm height connector)
- **BOOTLOADER AND OS SUPPORT** - Uboot and Linux 2.6.31+

3.2 BLOCK DIAGRAM

Refer to the following figure for a block diagram of the CSB1724 SOM.

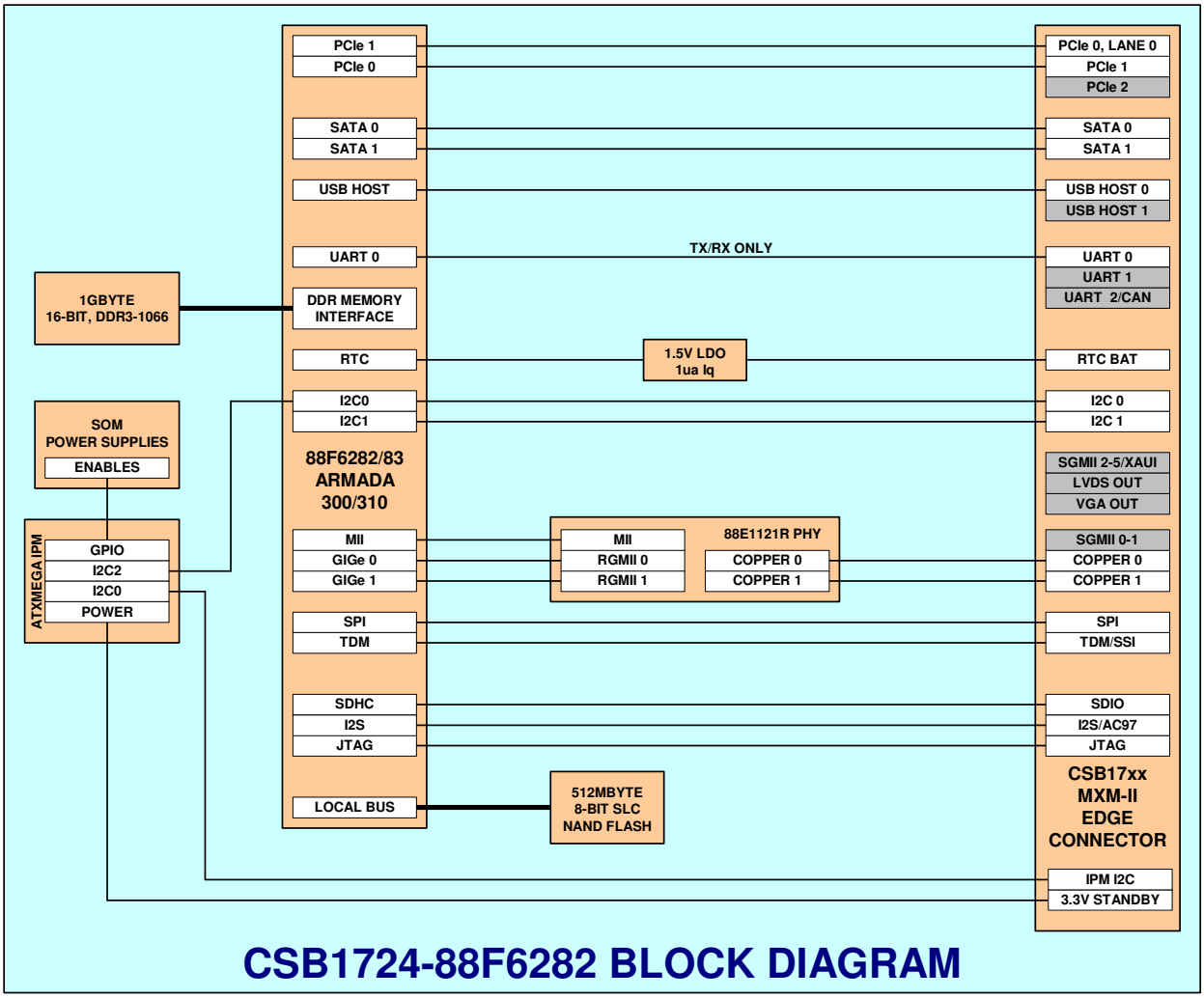

Figure 1 – CSB1724 Block Diagram

4 ON-BOARD DEVICES

4.1 CSB1724 ADDRESS MAP

The following table describes the Address Map of the CSB1724. Refer to the 88F6282 documentation for information regarding on-chip peripheral addressing.

CPU Chip Select	Chip Select Width	Base Address	Size	Description
*NF_CE	-	0xF800.0000	-	512MByte NAND
*MCS0	16	0x0000.0000	512MB	512Mbyte DDR3-1066 SDRAM
*MCS1	16	0x1000.0000	512MB	512Mbyte DDR3-1066 SDRAM

Table 2 – CSB1724 Address Map

4.2 512MBYTE DDR2-800 SDRAM

The CSB1724 uses four 256Mx8, DDR3-1066 SDRAM devices, 2 each connected to *MCS0 and *MCS1 for a total of 1Gbyte of system memory. The 88F6282 memory controller must be programmed for correct operation. Refer to the 88F6282 documentation for more information on programming the SDRAM Memory Controller.

4.3 512MBYTE 8-BIT NAND FLASH

The CSB1724 has a single 8-Bit, 512Mbyte NAND Flash. This device is connected to the 88F6282 device bus. The signals used to interface with the NAND Flash are shown in the following table.

NAND Signal	88F6282 Signal	Notes
*CE	*NF_CE	NAND Chip Select
*WE	*NF_WE	Write Strobe
*RE	*NF_RE	Read Strobe
ALE	NF_ALE	Addresses are latched on the rising edge of *WE when ALE = 1
CLE	NF_CLE	Commands are latched on the rising edge of *WE when CLE = 1

D0-1 D2-7	MPP18 - MPP19, MPP0 - MPP5	8-Bit Data bus. Addresses, Commands and Data are transferred via these signals

Table 3 – 88F6282 to NAND Flash Connections

4.3.1 NAND FLASH NOTES

1. The NAND Flash is the primary boot device. After boot *NF_CE should be programmed with optimal timing. Refer to the NAND documentation for more detail.
2. The Write Protect pin of the NAND Flash is tied high, so no HW Write Protect function is available.
3. At the time this document was written a Micron MT29F4G08ABADAWP, (4Gbit, 512M x 8, SLC) device was populated on the CSB1724. Future versions may ship with the same or larger capacity device. Contact Cogent for updated information on the currently shipping NAND Flash.

4.4 MARVELL 88E1121R DUAL PHY

The CSB1724 uses the 88E1121R to interface the two 88F6282 10/100/1000 Gigabit Ethernet Controllers to the system. The 88E1121R supports Twisted-Pair Copper. The signals used to interface the 88E1121R to the 88F6282 are shown in the following table.

88E1121R Signal	88F6282 Signal	Notes
P0_RXD[0:3]	GE0_RXD[0:3]	GIGe 0 Receive Data
P0_RX_CTL	GE0_RXDV	GIGe 0 Receive Data Valid strobe
P0_RX_CLK	GE0_RXCK	GIGe 0 Receive Clock
P0_TXD[0:3]	GE0_TXD[0:3]	GIGe 0 Transmit Data
P0_TX_CTL	GE0_TXEN	GIGe 0 Transmit Data Enable strobe
P0_TX_CLK	GE0_TXCLKOUT	GIGe 0 Transmit Clock
P0_MDC	GE_MDC	MII Bus Clock, PHY Address 0
P0_MDIO	GE_MDIO	MII Bus Data, PHY Address 0
P1_RXD[0:3]	GE1_RXD[0:3]/ MPP[24:27]	GIGe 1 Receive Data

P1_RX_CTL	GE1_RXCTL/ MPP30	GIGe 1 Receive Control
P1_RX_CLK	GE1_RXCK/ MPP31	GIGe 1 Receive Clock
P1_TXD[0:3]	GE1_TXD[0:3]/ MPP[20:23]	GIGe 1 Transmit Data
P1_TX_CTL	GE1_TXCTL/ MPP33	GIGe 1 Transmit Control
P1_TX_CLK	GE1_TXCK/ MPP32	GIGe 1 Transmit Clock
P1_MDC	-	88E1121R is configured for shared MDIO
P1_MDIO	-	88E1121R is configured for shared MDIO

Table 4 – 88F6282 to 88E1121R Connections

4.4.1 88E1121R INTERFACE NOTES

1. The Copper signals from the 88E1121R are routed to MXM ports GIGE0 and GIGE1. They are designed to connect to a 10/100/1000 compatible transformer (with the transformer center tap connected to GIGE_CTREF and bypassed to ground with a .1uf capacitor). These signals should be routed differentially (100 ohm impedance) and separated from other signals by at least 25mils. The total length from the carrier board MXM Connector to the transformer should be 4” or less.

2. 88E1121R LED outputs LED2, LED1 and LED0 must be programmed for Link 1GBIT, Link 100MBIT and Link any speed respectively. Additionally LED0 should also be programmed to blink during receive or transmit activity.

4.5 ICS9DB102 DIFFERENTIAL CLOCK BUFFER

The CSB1724 uses an ICS9DB102 Dual Differential Clock Buffer. The input is from the MXM PCIe Reference Clock Port. The outputs are 100Mhz CML Mode differential for 88F6282 PCI Express 0 and PCI Express 1 Reference Clock inputs.

4.6 ATTINY2313 IPM MICROCONTROLLER

The CSB1724 uses an Atmel ATTINY2313 8-bit Microcontroller to provide configuration, power sequencing and thermal management functions for the 88F6282. The ATTINY2313 is described in more detail in section 7.

5 88F6282 ON-CHIP PERIPHERALS

5.1 OVERVIEW

The 88F6282 has a number of on-chip peripheral devices as well as a number of user defined Multifunction Programmable Pins (MPP). While it is beyond the scope of this document to provide detailed programming and interfacing information for the 88F6282 on-chip peripherals, the following section describes the assignments for these peripherals and MPP's as they are implemented on the CSB1724.

5.2 88F6282 TO MXM PERIPHERAL MAPPING

The following table provides a high level view of the mapping from the various 88F6282 peripherals to the MXM ports. Due to pin multiplexing on the 88F6282, not all ports are available.

88F6282 Peripheral	MXM Port	Description and Notes
TDM	TDM/SSP	Time Domain Multiplexed Bus
TDM SPI or Audio I2S	I2S	Programmable as TDM SPI or I2S
SPI	-	Unavailable - Pins Used by NAND
TW0	I2C0	
TW1	I2C1	
LCD	-	LCD Port is not supported per Marvell errata
UART0	UART0	2-Wire TTL, TXD and RXD only
UART1	-	Unavailable - Pins used by SD/MMC port
USB	USBH0	480Mbit USB 2.0 Host Port
GIGe0	GIGE0	10/100/1000Mbit Copper Interface
GIGe1	GIGE1	10/100/1000Mbit Copper Interface
PCI Express 0	PCIe0, Lane 0	PCI Express x1
PCI Express 1	PCIe1	PCI Express x1

Table 5 – 88F6282 to MXM Port Mapping

5.3 88F6282 CHIP SELECTS

As described in Section 4.1, the 88F6282 Chip Selects are used to enable the various devices on the CSB1724.

5.4 88F6282 MULTI- PURPOSE PIN ASSIGNMENTS

The 88F6282 has 50 Multi- Purpose Pins (0 to 49). The usage on the CSB1724 is described in the following table. It is the responsibility of software to setup these bits for the correct direction and default state as well as the assignment of alternate functions.

88F6282 MPP	DIR	CSB1724 Usage	Description and Notes
0-5	I/O	NAND	NAND Data bits 2-7
6	OUT	*SYS_RST	System Reset Out from CPU
7	-	-	Unused
8	I/O	I2C0_SDA	Two-Wire Interface 0 Data
9	I/O	I2C0_SCL	Two-Wire Interface 0 Clock
10	OUT	U0_TXD	UART 0 Transmit Data
11	IN	U0_RXD	UART 0 Receive Data
12	OUT	SD_CLK	SD/MMC Clock
13	I/O	SD_CMD	SD/MMC Command
14-17	I/O	SD_D0-3	SD/MMC Data Bus
18-19	I/O	NAND	NAND Data bits 0-1
20-23	OUT	E1_TXD0-3	Gigabit Ethernet Port 1 Transmit Data 0-3
24-27	IN	E1_RXD0-3	Gigabit Ethernet Port 1 Receive Data 0-3
28	IN	*TDM_INT	TDM Codec Interrupt
29	OUT	*TDM_RST	TDM Codec Reset
30	IN	E1_RXCT	Gigabit Ethernet Port 1 Receive Control
31	IN	E1_RXCK	Gigabit Ethernet Port 1 Receive Clock
32	IN	E1_TXCK	Gigabit Ethernet Port 1 Transmit Clock
33	OUT	E1_TXCT	Gigabit Ethernet Port 1 Transmit Control
34	OUT	*SA0_ACT	SATA Port 0 Activity Indicator
35	OUT	*SA1_ACT	SATA Port 1 Activity Indicator

88F6282 MPP	DIR	CSB1724 Usage	Description and Notes
36	I/O	I2C1_SDA	Two-Wire Interface 1 Data
37	I/O	I2C1_SCL	Two-Wire Interface 1 Clock
38	I/O	*SD_CD	SD/MMC Card Detect – GPIO Mode
39	I/O	I2S_BCLK	I2S Bit Clock
40	OUT	I2S_DO	I2S Data Out (to Codec)
41	I/O	I2S_LRCLK	I2S Left/Right Clock
42	I/O	I2S_MCLK	I2S Master Clock
43	IN	I2S_DI	I2S Data In (from Codec)
44	IN	*PE_WAKE	Shared PCIe Wake from Port 0 and Port 1
45	OUT	TDM_CLK	TDM Clock
46	OUT	TDM_FS	TDM Frame Sync
47	IN	TDM_RXD	TDM Receive Data
48	OUT	TDM_TXD	TDM Transmit Data
49	IN	*I2C_INT	I2C Devices Shared Interrupt

Table 6 – 88F6282 MPP Pin Assignments

5.5 88F6282 UARTS

The 88F6282 has 2 UARTS. Due to pin multiplexing restrictions, only UART0 TXD and RXD are available. UART 0 is routed to the MXM Connector as shown in the following table. Refer to the 88F6282 documentation for more information about the 88F6282 UARTS.

88F6282 Signal	MXM Signal	Notes
U0_TXD/MPP10	U0_TXD	UART 0 Transmit
U0_RXD/MPP11	U0_RXD	UART 0 Receive

Table 7 – 88F6282 to MXM UART Connections

5.6 88F6282 I2C INTERFACES

The 88F6282 has two I2C Interfaces. Both are High Speed (100Khz/400Khz), master/slave I2C Serial Controllers. The 88F6282 I2C Controllers are routed to the

MXM Connector as shown in the following table. Refer to the 88F6282 documentation for detailed programming information on both I2C controllers.

88F6282 Signal	MXM Signal	Notes
TW0_SCL/MPP9	I2C0_SCL	I2C Bus 0 Clock
TW0_SDA/MPP8	I2C0_SDA	I2C Bus 0 Data
MPP49	*I2C0_INT	I2C Bus 0 Interrupt
TW1_SCL/MPP37	I2C1_SCL	I2C Bus 1 Clock
TW1_SDA/MPP36	I2C1_SDA	I2C Bus 1 Data

Table 8 – 88F6282 to MXM I2C Connections

5.7 88F6282 LOCAL BUS INTERFACE

The 88F6282 support an 8-bit Data bus for expansion use. The NAND Flash is connected to this bus on the CSB1724. This bus is not available off board. Refer to the 88F6282 documentation for detailed programming information on the Local Bus Interface.

5.8 88F6282 PCI EXPRESS PORTS

The 88F6282 supports 2 PCI Express Ports, one lane each. Refer to the 88F6282 documentation for detailed programming information on the PCI Express Controllers.

5.8.1 88F6282 PCI EXPRESS INTERFACE NOTES

1. The controllers may be defined at configuration time as root ports or endpoints individually.
2. The optional PCI Express wakeup signal for both ports is connected to MPP44.

5.9 88F6282 USB CONTROLLER

The 88F6282 has one 480Mbit, USB 2.0 Port. It is routed to MXM Port USBH0. Refer to the 88F6282 documentation for detailed programming information on the USB Controller.

6 CSB1724 CLOCKING

6.1 88F6282 INPUT CLOCKS

The 88F6282 is provided with several input clocks as described in the following table.

CLOCK	Description and Notes
REF_CLK_XIN	25Mhz clock. Used by the 88F6282 to create its core clock, as well as the DDR clock, Platform and Local Bus clocks.
RTC_XIN/XOUT	32.768Khz clock. Used by the 88F6282 to create its real time clock.
PEX0_REF_CLK	100Mhz differential clock from ICS9DB102 Differential Clock Buffer. Used as reference clock for 88F6282 PCI Express 0.
PEX1_REF_CLK	100Mhz differential clock from ICS9DB102 Differential Clock Buffer. Used as reference clock for 88F6282 PCI Express 1.

Table 9 – 88F6282 Input Clocks

6.2 88F6282 OUTPUT CLOCKS

The 88F6282 drives several output clocks as described in the following table. Note that the output frequency of M_CLK is defined during configuration. The rest must be defined by software, equal to or less than the listed maximum frequency.

CLOCK	Description and Notes
M_CLK	Differential Memory Clock, 400Mhz
SD_CLK	SD/MMC up to 50Mhz
I2S_CLK	I2S Audio Clock, 12.288Mhz
I2C0_SCL	I2C Bus 1 Clock up to 400Khz
I2C1_SCL	I2C Bus 2 Clock up to 400Khz

Table 10 – 88F6282 Output Clocks

6.3 88E1121R CLOCK

The 88E1121R is supplied with a 25Mhz reference clock.

7 CSB1724 POWER MANAGEMENT

7.1 OVERVIEW

The CSB1724 has a sophisticated power management mechanism using an Atmel ATTINY2313 8-bit Microcontroller.

7.2 ATTINY2313 IPM MICROCONTROLLER

The ATTINY2313 8-bit Microcontroller is used to provide the following features: power supply sequencing; 88F6282 configuration; clock PLL programming; 88F6282 power sequencing; and off-board power supply control. The ATTINY2313 uses a number of internal peripherals and GPIO's to perform these tasks. The following table lists the ATTINY2313 signals and peripherals used on the CSB1724.

ATTINY 2313 Port	DIR	CSB1724 Usage	Description and Notes
PA0	OUT	*V33_EN	3.3V Regulator Enable
PA1	IN	V33_PG	3.3V Regulator Power Good
PA2	IN	*IPM_RST	Reset Input
PB0	-	-	Unused
PB1	OUT	VD_EN	88F6282 Platform Voltage Regulator Enable
PB2	OUT	V15_EN	1.5V Regulator Enable
PB3	OUT	VC_EN	88F6282 Core Voltage Regulator Enable
PB4	IN	CPU_SEL	0 = Select 88F6283 – Currently unused
PB5	I/O	IPM_SDA	IPM I2C Bus Data to/from MXM. Used to control target power supply and read configuration Switches
PB6	I/O	IPM_DBG	IPM Debug Bit
PB7	I/O	IPM_SCL	IPM I2C Clock to/from MXM. Used to control target power supply and read configuration Switches
PD0	I/O	I2C1_SDA	I2C Data to Configuration Expanders
PD1	I/O	I2C1_SCL	I2C Data to Configuration Expanders
PD2	IN	*RST_IN	MXM Reset In
PD3	-	-	Unused

ATTINY 2313 Port	DIR	CSB1724 Usage	Description and Notes
PD4	IN	*SYS_RST	System Reset from 88F6282
PD5	OUT	*POR	Power On Reset to the 88F6282
PD6	I/O	*IPM_INT	IPM I2C Bus Interrupt/Alert. Currently unused.

Table 11 – ATTINY2313 Peripheral and GPIO usage

7.2.1 ATTINY2313 MICROCONTROLLER NOTES

3. All information regarding the pinout, usage and presence of the ATTINY2313 is subject to change and is provided for informational purposes only.
4. Future versions of the CSB1724 may use other versions of the ATTINY family or even different IPM Microcontrollers altogether.
5. The ATTINY2313 provides configuration strapping to the 88F6282 via two on-board I2C registers. The 88F6282 configuration process is described in detail in section 8.

7.3 IPM CONFIGURATION INTERFACE

The ATTINY2313 software probes for the presence of a PCA9554 located on the IPM I2C Bus at address 0x27. It is used to read an 8-bit value to determine the proper configuration of the CSB1724. This can be a switch, header with jumpers, or hard-wired on the target board. The bit assignments for the CSB1724 are shown in the following table.

PCA9554 Bit	Name	Description and Notes

PCA9554 Bit	Name	Description and Notes
0	CFG_FREQ	88F6282: 1 = Core Clock is 1.6Ghz, DDR Clock Ratio is 4:1. L2 Clock Ratio is 4:1 0 = Core Clock is 1.2Ghz, DDR Clock Ratio is 3:1. L2 Clock Ratio is 3:1 88F6283: 1 = Core Clock is 800Mhz, DDR Clock Ratio is 2:1. L2 Clock Ratio is 2:1 0 = Core Clock is 600Mhz, DDR Clock Ratio is 2:1. L2 Clock Ratio is 2:1
2:1	CFG_BOOT	11 = NAND 10 = SATA 01 = SPI 00 = PCIe0
3	RFU	Reserved for Future Use
4	RFU	Reserved for Future Use
5	RFU	Reserved for Future Use
6	RFU	Reserved for Future Use
7	RFU	Reserved for Future Use

Table 12 – IPM Configuration Interface Bit Assignments

7.3.1 IPM CONFIGURATION INTERFACE NOTES

1. If the probe fails, the ATTINY2313 assumes all values are 1.
2. The ATTINY2313 reads this value whenever it resets the 88F6282, not just at power up.
3. The ATTINY2313 reads the value on Port Pin PR0 to determine the installed CPU. A 0 = indicates the 88F6283 and a 1 indicates the 88F6282. This option is currently unsupported.

7.4 IPM POWER SUPPLY INTERFACE

The ATTINY2313 software probes for a PCA9536 located on the IPM I2C Bus at address 0x41. This 4-bit expander is used to interface the CSB1724 with an ATX style

power supply. The bit assignments are shown in the following table.

PCS9536 Bit	Name	Description and Notes
0	*PWR_SW	Low True Power On/Off Switch
1	*PS_ON	Low True Power On to Power Supply
2	PS_OK	High True Power OK from Power Supply
3	IPM_LED	Low True LED Enable for IPM Use

Table 13 – IPM Power Supply Interface Bit Assignments

7.4.1 IPM POWER SUPPLY INTERFACE NOTES

1. If the probe fails, the ATTINY2313 operates in “Always On Mode 0”. The ATTINY2313 will power up the CSB1724 as soon as VIN reaches the minimum to operate.
2. The ATTINY2313 software monitors the *PWR_SW signal after power up. If it is always low, the ATTINY2313 operates in “Always On Mode 1”. It will sequence the target power supply, then power up the CSB1724.
3. If the PCA9536 is present, the ATTINY2313 will enable the IPM_LED at its own reset. The IPM_LED stays on until the ATTINY2313 has completed powering up the CSB1724, thus providing an indication of successful power up.

8 88F6282 CONFIGURATION

8.1 OVERVIEW

When it's *SYSRST input is released, the 88F6282 samples a number of pins to set various configuration options. These options and the pins used are detailed in the following table. Refer to the 88F6282 documentation for more information on the overall configuration options.

8.2 DEFAULT CONFIGURATION

The following table lists the configuration pins and the values driven on the CSB1724. Values that are driven by the ATTINY2313 are shown with a "Y" in the IPM column.

88F6282 PIN	Name	IPM	Description and Notes
MPP1	TWSI0 ROM INIT	N	0, no I2C INIT
MPP2, MPP5, MPP19, MPP10	CPU_FREQ	Y	88F6282: 0x9 = 1200Mhz 0xD = 1600Mhz 0xE = 1800Mhz (unsupported) 0xF = 2000Mhz (unsupported) 88F6283: 0x4 = 600Mhz 0x6 = 800Mhz 0x7 = 1000Mhz (unsupported)
MPP33, NF_ALE, *NF_RE, NF_CLE	CPU_DDR_RATIO	Y	88F6282: 0x4 = 3:1 0x6 = 4:1 0x8 = 5:1 88F6283: 0x1 = 2:1 0x3 = 2.5:1

88F6282 PIN	Name	IPM	Description and Notes
MPP3, MPP12, *NF_WE	CPU_L2_RATIO	Y	88F6282: 0x3 = 3:1 0x5 = 4:1 88F6283: 0x1 = 2:1 0x3 = 3:1
GE_TXD[2:0]	BOOT	Y	0x2 = Boot from SPI flash (SPI_CSn on MPP[7]) 0x4 = Boot from SPI flash (SPI_CSn on MPP[0]) 0x5 = Boot from NAND Flash 0x6 = Boot from SATA 0x7 = Boot from PCI Express port 0
GE_MDC	PEX0_CLK	N	0, PCIe 0 reference clock is input
MPP49	PEX1_CLK	N	0, PCIe 1 reference clock is input
GE_TXD2	SSCG	N	1, Disable Spread Spectrum Clock
MPP18	TCLK_FREQ	N	0, 200Mhz TCLK

Table 14 – 88F6282 Configuration Settings

9 CSB1724 SOFTWARE

9.1 OVERVIEW

Due to the various resources contained on the CSB1724, both internal and external to the 88F6282, it is necessary to initialize a large number of 88F6282 registers and external devices before correct operation can begin. These values and their proper sequencing are beyond the scope of this document. Contact Cogent for example boot initialization code.

10 MXM FORMAT/PINOUT

10.1 OVERVIEW

This section provides an introduction to the Cogent MXM form factor as well as the pinout of the MXM edge connector on the CSB1724.

10.2 MXM FORMAT

The CSB1724 is fully compatible with the Cogent CSB17xx family of Cogent MXM SOM (System On a Module) boards. Although this form factor uses the low cost, high performance MXM II connector developed originally for laptop computer graphics cards, the Cogent MXM SOM form factor, pinout and pin orientation are not related to, nor compatible with, any other form factor. The layout of the CSB1724 is shown in the following figures (for illustrative purposes only)

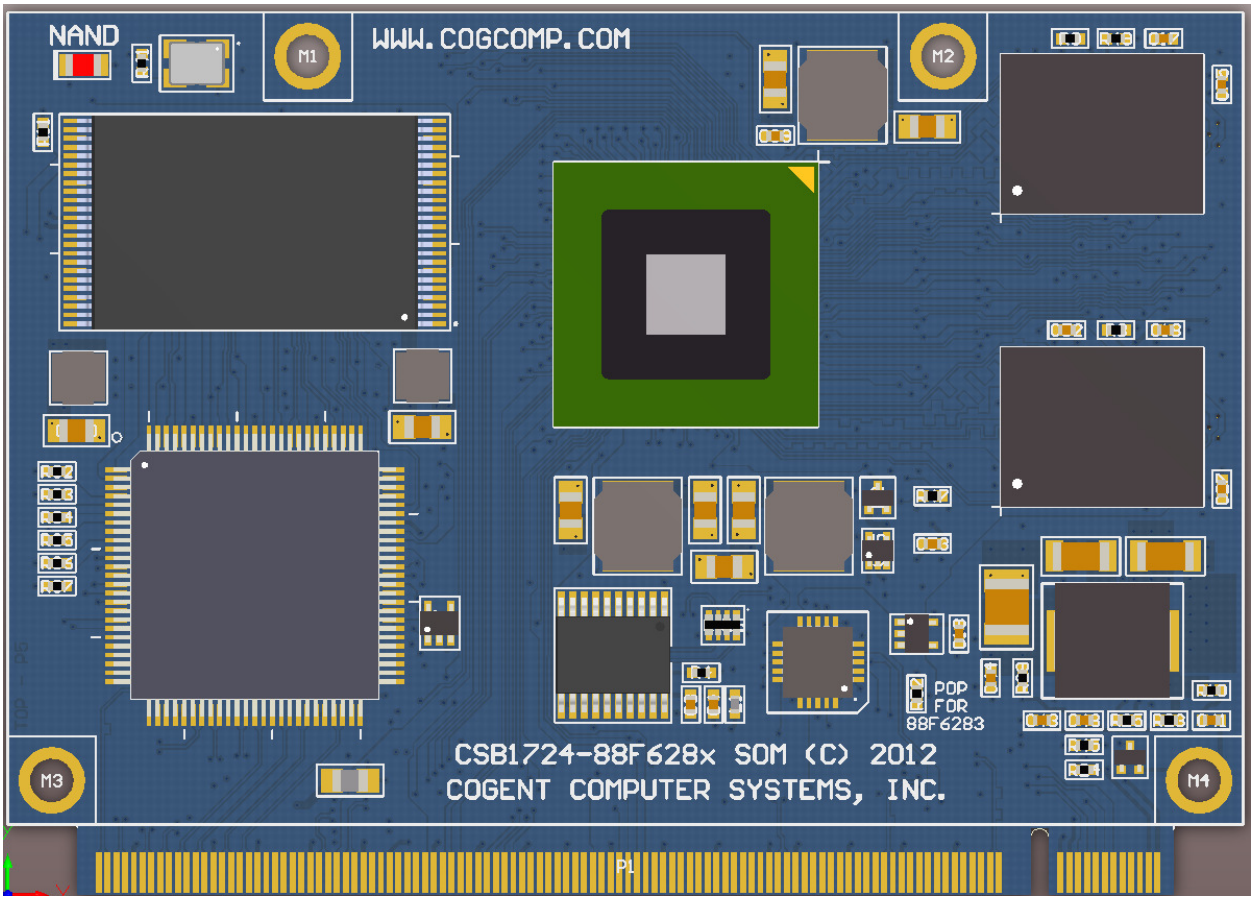

Figure 2 – CSB1724 Top Side Placement

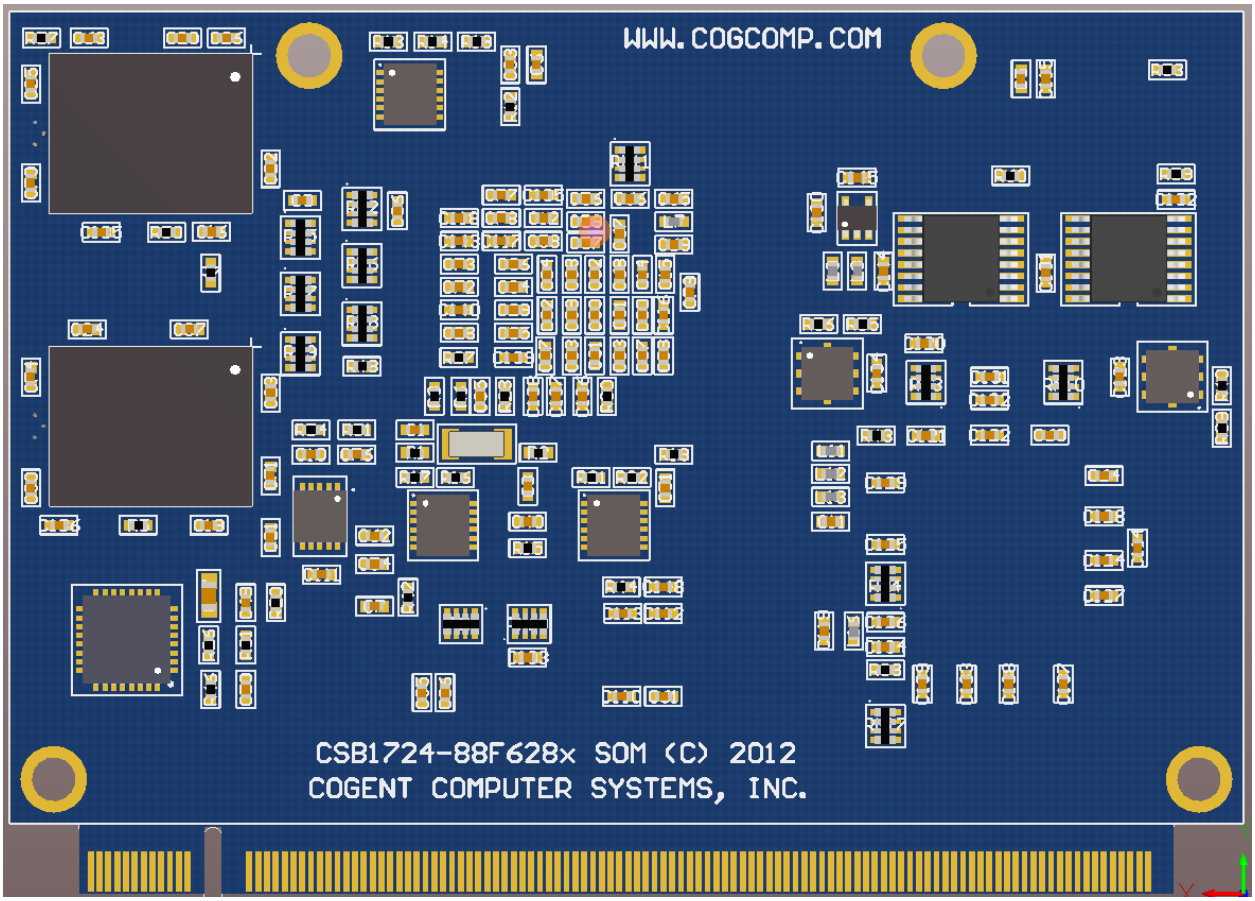

Figure 3 – CSB1724 Bottom Side Placement

10.3 MXM CONNECTOR

The MXM format is an edge card with two sides, A and B. Each side has 115 contacts for a total of 230-pins. The MXM connector is available from multiple vendors and with differing stack heights. Vendor part numbers for this are shown in the following table.

Vendor	Part Number	Connector Height	Board-Board Spacing
Foxconn	AS0B326-S78N-7F	7.8mm	5mm
Foxconn	AS0B326-S55N-7F	5.5mm	2.7mm
Foxconn	AS0B326-S43N-7F	4.3mm	1.5mm
Genesis Technology	GTI08-30375	7.8mm	5mm
ACES	88882-2Dxx	7.8mm	5mm
ACES	88885-2Dxx	5.5mm	2.7mm

Table 15 – CSB1724 Connector to Mated Height

10.3.1 MXM CONNECTOR NOTES

4. The board-board value refers to the spacing between the bottom side of the CSB1724 PCB and the top surface of the carrier board.
5. The maximum height of any component on the bottom side of the CSB1724 is 1.2mm.
6. The maximum height of any component on the top side (excluding heat spreaders or heat sinks) is 3mm.
7. The thickness of the CSB1724 PCB is 1.2mm.

10.4 MXM CONNECTOR PINOUTS

The CSB1724 uses 230 edge fingers to mate with a standard MXM-II socket. The following tables describe the pinout of these connectors. An "N" in the column marked CSB indicates that the signal is not supported by the CSB1724. Power signals are shown in bold. This pinout conforms to the "Network" variant of the Cogent MXM SOM standard.

MXM CONNECTOR PINOUT			
PIN	**NAME**	**CSB**	**CSB1724 USAGE AND NOTES**
A1	**GE0_MDI_0_M**		GIGE 0 MDI 0 MINUS
B1	***GE1_SPD1G**		GIGE 1 SPEED 1GBIT LED OUT
A2	**GE0_MDI_0_P**		GIGE 0 MDI 0 PLUS
B2	***GE0_SPD1G**		GIGE 0 SPEED 1GBIT LED OUT
A3	**GE0_MDI_1_M**		GIGE 0 MDI 1 MINUS
B3	***GE1_LNK**		GIGE 1 LINK/ACTIVITY LED OUT
A4	**GE0_MDI_1_P**		GIGE 0 MDI 1 PLUS
B4	***GE0_LNK**		GIGE 0 LINK/ACTIVITY LED OUT
A5	**VCC3**		**3.3V OUTPUT**
B5	**VCC3**		**3.3V OUTPUT**
A6	**GE0_MDI_2_M**		GIGE 0 MDI 2 MINUS
B6	***GE1_SPD100**		GIGE 1 SPEED 100MBIT LED OUT
A7	**GE0_MDI_2_P**		GIGE 0 MDI 2 PLUS
B7	***GE0_SPD100**		GIGE 0 SPEED 100MBIT LED OUT

MXM CONNECTOR PINOUT			
PIN	**NAME**	**CSB**	**CSB1724 USAGE AND NOTES**
A8	**GE0_MDI_3_M**		GIGE 0 MDI 3 MINUS
B8	**MDIO**		MII BUS DATA FOR EXTERNAL PHYS
A9	**GE0_MDI_3_P**		GIGE 0 MDI 3 PLUS
B9	**MDC**		MII BUS CLOCK FOR EXTERNAL PHYS
A10	**GE1_MDI_3_M**		GIGE 1 MDI 3 MINUS
B10	***MII_INT**		MII BUS INTERRUPT IN FROM EXTERNAL PHYS
A11	**GE1_MDI_3_P**		GIGE 1 MDI 3 PLUS
B11	***I2C0_INT**		PRIMARY I2C BUS INTERRUPT IN
A12	**GE1_MDI_2_M**		GIGE 1 MDI 2 MINUS
B12	**I2C0_SCL**		PRIMARY I2C BUS CLOCK
A13	**GE1_MDI_2_P**		GIGE 1 MDI 2 PLUS
B13	**I2C0_SDA**		PRIMARY I2C BUS DATA
A14	**GND**		**GROUND**
B14	**GND**		**GROUND**
A15	**GE1_MDI_1_M**		GIGE 1 MDI 1 MINUS
B15	**GE0_CTREF**		GIGE CENTER TAP REFERENCE VOLTAGE
A16	**GE1_MDI_1_P**		GIGE 1 MDI 1 PLUS
B16	**GE_CTREF**		ALWAYS CONNECT TO B15
A17	**GE1_MDI_0_M**		GIGE 1 MDI 0 MINUS
B17	**I2C1_SCL**		SECONDARY I2C BUS CLOCK
A18	**GE1_MDI_0_P**		GIGE 1 MDI 0 PLUS
B18	**I2C1_SDA**		SECONDARY I2C BUS DATA
A19	**VCC3**		**3.3V OUTPUT**
B19	**VCC3**		**3.3V OUTPUT**
A20	**SG1_TD_M**	N	SGMII 1 TRANSMIT MINUS
B20	**SG1_RD_M**	N	SGMII 1 RECEIVE MINUS
A21	**SG1_TD_P**	N	SGMII 1 TRANSMIT PLUS

MXM CONNECTOR PINOUT			
PIN	**NAME**	**CSB**	**CSB1724 USAGE AND NOTES**
B21	**SG1_RD_P**	N	SGMII 1 RECEIVE PLUS
A22	**SG1_SD**	N	SGMII 1 SIGNAL DETECT
B22	**SG0_SD**	N	SGMII 0 SIGNAL DETECT
A23	**SG0_TD_M**	N	SGMII 0 TRANSMIT MINUS
B23	**SG0_RD_M**	N	SGMII 0 RECEIVE MINUS
A24	**SG0_TD_P**	N	SGMII 0 TRANSMIT PLUS
B24	**SG0_RD_P**	N	SGMII 0 RECEIVE PLUS
A25	**GND**		**GROUND**
B25	**GND**		**GROUND**
A26	**SA1_TD_M**		CPU SATA 1 TRANSMIT MINUS
B26	**SA1_RD_M**		CPU SATA 1 RECEIVE MINUS
A27	**SA1_TD_P**		CPU SATA 1 TRANSMIT PLUS
B27	**SA1_RD_P**		CPU SATA 1 RECEIVE PLUS
A28	***SA1_ACT**		SATA 1 ACTIVITY
B28	***SA0_ACT**		SATA 0 ACTIVITY
A29	**SA0_TD_M**		CPU SATA 0 TRANSMIT MINUS
B29	**SA0_RD_M**		CPU SATA 0 RECEIVE MINUS
A30	**SA0_TD_P**		CPU SATA 0 TRANSMIT PLUS
B30	**SA0_RD_P**		CPU SATA 0 RECEIVE PLUS
A31	**VCC3**		**3.3V OUTPUT**
B31	**VCC3**		**3.3V OUTPUT**
A32	**UH1_M**	N	USB HOST PORT 1 MINUS
B32	**UH0_M**		USB HOST PORT 0 MINUS
A33	**UH1_P**	N	USB HOST PORT 1 PLUS
B33	**UH0_P**		USB HOST PORT 0 PLUS
A34	**GND**		**GROUND**
B34	**GND**		**GROUND**

MXM CONNECTOR PINOUT			
PIN	**NAME**	**CSB**	**CSB1724 USAGE AND NOTES**
A35	**VGA_R**	N	ANALOG VGA RED
B35	**VGA_HS**	N	ANALOG VGA HORIZONTAL SYNC
A36	**VGA_G**	N	ANALOG VGA GREEN
B36	**VGA_VS**	N	ANALOG VGA VERTICAL SYNC
A37	**VGA_B**	N	ANALOG VGA BLUE
B37	**I2S_MCLK**		I2S MASTER CLOCK
A38	***TDM_INT**		TDM INTERRUPT IN
B38	***TDM_RST**		TDM RESET OUT
A39	**VCC3**		**3.3V OUTPUT**
B39	**VCC3**		**3.3V OUTPUT**
A40	**MC_CLK**		SD/MMC CLOCK
B40	**MC_CS_D3**		SD/MMC DATA 3 (SPI CS)
A41	**MC_DIN_CMD**		SD/MMC COMMAND (SPI MOSI)
B41	**MC_DOUT_D0**		SD/MMC DATA 0 (SPI MISO)
A42	**MC_IRQ_D1**		SD/MMC DATA 1 (SPI/SDIO IRQ)
B42	**MC_D2**		SD/MMC DATA 2
A43	**MC_WP**		SD/MMC WRITE PROTECT
B43	***MC_CD**		SD/MMC DETECT
A44	**GND**		**GROUND**
B44	**GND**		**GROUND**
A45	**I2S_BCLK**		I2S BIT CLOCK
B45	**I2S_LRCLK**		I2S LEFT/RIGHT CLOCK
A46	**I2S_TXD**		I2S TRANSMIT DATA
B46	**I2S_RXD**		I2S RECEIVE DATA
A47	**TDM_CLK**		TDM CLOCK
B47	**TDM_FS**		TDM FRAME SYNC
A48	**TDM_TXD**		TDM TRANSMIT DATA

MXM CONNECTOR PINOUT			
PIN	**NAME**	**CSB**	**CSB1724 USAGE AND NOTES**
B48	**TDM_RXD**		TDM RECEIVE DATA
A49	**VCC3**		**3.3V OUTPUT**
B49	**VCC3**		**3.3V OUTPUT**
A50	**SPI_CLK**	N	SPI CLOCK
B50	***SPI_CS**	N	SPI CHIP SELECT
A51	**SPI_MOSI**	N	SPI MASTER OUT, SLAVE IN
B51	**SPI_MISO**	N	SPI MASTER IN, SLAVE OUT
A52	**U2_TXD**	N	UART 2 TRANSMIT
B52	**U2_RXD**	N	UART 2 RECEIVE
A53	**U2_RTS**	N	UART 2 CLEAR TO SEND
B53	**U2_CTS**	N	UART 2 REQUEST TO SEND
A54	**GND**		**GROUND**
B54	**GND**		**GROUND**
A55	**U1_TXD**	N	UART 1 TRANSMIT
B55	**U1_RXD**	N	UART 1 RECEIVE
A56	**U1_RTS**	N	UART 1 CLEAR TO SEND
B56	**U1_CTS**	N	UART 1 REQUEST TO SEND
A57	**U0_TXD**		UART 0 TRANSMIT
B57	**U0_RXD**		UART 0 RECEIVE
A58	**U0_RTS**	N	UART 0 CLEAR TO SEND
B58	**U0_CTS**	N	UART 0 REQUEST TO SEND
A59	**VCC3**		**3.3V OUTPUT**
B59	**VCC3**		**3.3V OUTPUT**
A60	***RST_IN**		SOM RESET IN
B60	***RST_OUT**		SOM RESET OUT
A61	***TRST**		JTAG RESET
B61	**TCK**		JTAG CLOCK

MXM CONNECTOR PINOUT			
PIN	**NAME**	**CSB**	**CSB1724 USAGE AND NOTES**
A62	**TMS**		JTAG MODE
B62	**TDI**		JTAG DATA IN
A63	**TDO**		JTAG DATA OUT
B63	**DBG0**	N	DEBUG SIGNAL 0
A64	**DBG1**	N	DEBUG SIGNAL 1
B64	**DBG2**	N	DEBUG SIGNAL 2
A65	**GND**		**GROUND**
B65	**GND**		**GROUND**
A66	**SD3_TD_M**	N	CPU SERDES 3 TRANSMIT MINUS
B66	**SD3_RD_M**	N	CPU SERDES 3 RECEIVE MINUS
A67	**SD3_TD_P**	N	CPU SERDES 3 TRANSMIT PLUS
B67	**SD3_RD_P**	N	CPU SERDES 3 RECEIVE PLUS
A68	**SD3_IO**	N	CPU SERDES 3 I/O
B68	**SD2_IO**	N	CPU SERDES 2 I/O
A69	**SD2_TD_M**	N	CPU SERDES 2 TRANSMIT MINUS
B69	**SD2_RD_M**	N	CPU SERDES 2 RECEIVE MINUS
A70	**SD2_TD_P**	N	CPU SERDES 2 TRANSMIT PLUS
B70	**SD2_RD_P**	N	CPU SERDES 2 RECEIVE PLUS
A71	**VCC3**		**3.3V OUTPUT**
B71	**VCC3**		**3.3V OUTPUT**
A72	**SD1_TD_M**	N	CPU SERDES 1 TRANSMIT MINUS
B72	**SD1_RD_M**	N	CPU SERDES 1 RECEIVE MINUS
A73	**SD1_TD_P**	N	CPU SERDES 1 TRANSMIT PLUS
B73	**SD1_RD_P**	N	CPU SERDES 1 RECEIVE PLUS
A74	**SD1_IO**	N	CPU SERDES 1 I/O
B74	**SD0_IO**	N	CPU SERDES 0 I/O
A75	**SD0_TD_M**	N	CPU SERDES 0 TRANSMIT MINUS

MXM CONNECTOR PINOUT			
PIN	**NAME**	**CSB**	**CSB1724 USAGE AND NOTES**
B75	**SD0_RD_M**	N	CPU SERDES 0 RECEIVE MINUS
A76	**SD0_TD_P**	N	CPU SERDES 0 TRANSMIT PLUS
B76	**SD0_RD_P**	N	CPU SERDES 0 RECEIVE PLUS
A77	**GND**		**GROUND**
B77	**GND**		**GROUND**
A78	**REF_CLK_M**		PCI EXPRESS REFERENCE CLOCK IN MINUS
B78	**LV_CK_M**	N	LVDS CLOCK OUT MINUS
A79	**REF_CLK_P**		PCI EXPRESS REFERENCE CLOCK IN PLUS
B79	**LV_CK_P**	N	LVDS CLOCK OUT PLUS
A80	**VCC3**		**3.3V OUTPUT**
B80	**VCC3**		**3.3V OUTPUT**
A81	**LV_D3_M**	N	LVDS DATA 3 OUT MINUS
B81	**LV_D2_M**	N	LVDS DATA 2 OUT MINUS
A82	**LV_D3_P**	N	LVDS DATA 3 OUT PLUS
B82	**LV_D2_P**	N	LVDS DATA 2 OUT PLUS
A83	**LCD_PWM**	N	LCD BRIGHTNESS PWM CONTROL OUT
B83	**LCD_BKL**	N	LCD BACKLIGHT POWER ENABLE OUT
A84	**LV_D1_M**	N	LVDS DATA 1 OUT MINUS
B84	**LV_D0_M**	N	LVDS DATA 0 OUT MINUS
A85	**LV_D1_P**	N	LVDS DATA 1 OUT PLUS
B85	**LV_D0_P**	N	LVDS DATA 0 OUT PLUS
A86	**GND**		**GROUND**
B86	**GND**		**GROUND**
A87	**PE2_TD_M**	N	PCI EXPRESS LINK 2, TRANSMIT MINUS
B87	**PE2_RD_M**	N	PCI EXPRESS LINK 2, RECEIVE MINUS
A88	**PE2_TD_P**	N	PCI EXPRESS LINK 2, TRANSMIT PLUS
B88	**PE2_RD_P**	N	PCI EXPRESS LINK 2, RECEIVE PLUS

MXM CONNECTOR PINOUT			
PIN	**NAME**	**CSB**	**CSB1724 USAGE AND NOTES**
A89	**PE1_DIR**	N	PCI EXPRESS LINK 1 DIRECTION
B89	***PE1_WAKE**		PCI EXPRESS LINK 1 WAKEUP
A90	**PE1_TD_M**		PCI EXPRESS LINK 1, TRANSMIT MINUS
B90	**PE1_RD_M**		PCI EXPRESS LINK 1, RECEIVE MINUS
A91	**PE1_TD_P**		PCI EXPRESS LINK 1, TRANSMIT PLUS
B91	**PE1_RD_P**		PCI EXPRESS LINK 1, RECEIVE PLUS
A92	**VCC3**		**3.3V OUTPUT**
B92	**VCC3**		**3.3V OUTPUT**
A93	**PE0_TD3_M**	N	PCI EXPRESS LINK 0, LANE 3 TRANSMIT MINUS
B93	**PE0_RD3_M**	N	PCI EXPRESS LINK 0, LANE 3 RECEIVE MINUS
A94	**PE0_TD3_P**	N	PCI EXPRESS LINK 0, LANE 3 TRANSMIT PLUS
B94	**PE0_RD3_P**	N	PCI EXPRESS LINK 0, LANE 3 RECEIVE PLUS
A95	**RSVD**	N	RESERVED
B95	**RSVD**	N	RESERVED
A96	**PE0_TD2_M**	N	PCI EXPRESS LINK 0, LANE 2 TRANSMIT MINUS
B96	**PE0_RD2_M**	N	PCI EXPRESS LINK 0, LANE 2 RECEIVE MINUS
A97	**PE0_TD2_P**	N	PCI EXPRESS LINK 0, LANE 2 TRANSMIT PLUS
B97	**PE0_RD2_P**	N	PCI EXPRESS LINK 0, LANE 2 RECEIVE PLUS
A98	**GND**		**GROUND**
B98	**GND**		**GROUND**
A99	**PE0_TD1_M**	N	PCI EXPRESS LINK 0, LANE 1 TRANSMIT MINUS
B99	**PE0_RD1_M**	N	PCI EXPRESS LINK 0, LANE 1 RECEIVE MINUS
A100	**PE0_TD1_P**	N	PCI EXPRESS LINK 0, LANE 1 TRANSMIT PLUS
B100	**PE0_RD1_P**	N	PCI EXPRESS LINK 0, LANE 1 RECEIVE PLUS
A101	**PE0_DIR**	N	PCI EXPRESS LINK 0 DIRECTION
B101	***PE0_WAKE**		PCI EXPRESS LINK 0 WAKEUP
A102	**PE0_TD0_M**		PCI EXPRESS LINK 0, LANE 0 TRANSMIT MINUS

MXM CONNECTOR PINOUT			
PIN	**NAME**	**CSB**	**CSB1724 USAGE AND NOTES**
B102	**PE0_RD0_M**		PCI EXPRESS LINK 0, LANE 0 RECEIVE MINUS
A103	**PE0_TD0_P**		PCI EXPRESS LINK 0, LANE 0 TRANSMIT PLUS
B103	**PE0_RD0_P**		PCI EXPRESS LINK 0, LANE 0 RECEIVE PLUS
A104	**GND**		**GROUND**
B104	**GND**		**GROUND**
A105	**VCC3**		**3.3V OUTPUT**
B105	**VCC3**		**3.3V OUTPUT**
A106	**IPM_SCL**		IPM MICRO I2C BUS CLOCK
B106	**VIN**		SOM POWER IN
A107	**IPM_SDA**		IPM MICRO I2C BUS DATA
B107	**VIN**		SOM POWER IN
A108	***IPM_INT**		IPM MICRO INTERRUPT
B108	**VIN**		SOM POWER IN
A109	***IPM_RST**		IPM MICRO RESET
B109	**VIN**		SOM POWER IN
A110	**IPM_DBG**		IPM MICRO DEBUG
B110	**VIN**		SOM POWER IN
A111	**IPM_RFU**		RESERVED FOR FUTURE IPM USE
B111	**VIN**		SOM POWER IN
A112	**FAN**	N	CPU FAN CONTROL
B112	**VIN**		SOM POWER IN
A113	**TACH**	N	CPU FAN SPEED
B113	**VIN**		SOM POWER IN
A114	**VCC3_SB**		POWER TO IPM DEVICES
B114	**VIN**		SOM POWER IN
A115	**RTC_BAT**		RTC BATTERY BACKUP POWER
B115	**VIN**		SOM POWER IN

Table 16 – CSB1724 MXM Connector Pinout

11 DOCUMENT REVISIONS

Date	Revision	Change
8/22/2011	P3.0	First Release
1/26/2012	P5.0	Major revision to reflect P5 PCB
3/26/2012	P6.0	Clarify MXM signal directions

Table 17 – Document Revisions